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Temperature influences of the interfacial layer in MOS (Pt/TiO_2/Si) structures

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Abstract

In this paper present *I-V* and *C-V* electrical characteristics of MOS (Pt/TiO_2/Si) were reported. In the *I-V* characteristics the various electric parameter estimated such as the ideality factor (n), barrier height (Φ_B), leakage current (I_c) and saturation current (I_o) were estimated and further analyzed with Cheung functions.

These electrical parameters were observed to be varying with heat treatment. The *C-V* characteristics, flat band voltage (V_{FB}), interface trap density (D_{it}), effective charge density (N_{eff}) and oxide trapped charge (Q_{ot}) were estimated and analyzed. The variation of these values with annealing temperature was correlated with restructuring and rearrangement of TiO_2/SiO_2 atoms at the metal/silicon interface. The hysteresis loop in counter clock wise voltage between -1 V to 1 V at 1 MHz frequency, after 600 °C heat treatment show the strong accumulation region, this may be due to the reduced interface trapped charge and dangling bond.

Keywords: Leakage current, Ideality factor, Flat band voltage, Oxide trapped charge

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1. Introduction

The band gap of SiO_2 about 9 eV and trap density of the bulk material is low, so that current passing through dielectric layer low. These oxide thickness increase with decreasing leakage current density. Other oxide materials with higher dielectric constant are suitable for optimising the leakage current, trap density and dangling bonds. Titanium dioxide (TiO_2) many interesting properties and various applications, such as in photo-catalytic activity, gas sensing, gate insulator and solar cells. TiO_2 thin films deposited on silicon/SiO_2 surface is very simple and significant role in all semiconductor devices. However, TiO_2 as a gate insulator shows higher leakage current due to higher band gap and high band offset than SiO_2 and silicon substrate. The anatase phase can be obtained at a temperature of 350 °C and it undergoes phase transformation to the more stable rutile phase at a higher temperature of 800 °C [1]. The phase transformation, from amorphous to crystalline anatase, can take place in the deposited films after annealing due to changes in grain boundary, packing density and defects [2, 3]. The TiO_2 thin films have been deposited using wide variety of techniques, like CVD [4], radio-frequency sputtering [5], atomic layer deposition [6], Sol-gel [7], Sputtering [8], pulsed laser deposition [9,] and spray pyrolysis [10, 11]. Among all the aforementioned methods of TiO_2 film synthesis, spray pyrolysis is quite widespread used technique due to its simplicity, commercial viability, potential for cost-effective, mass production and easier usage. The MOS structures constitute a kind of capacitor, which stores the electric charge by virtue of the dielectric property of insulating layers. Due to the presence of oxide layer and two surface-charge regions, MOS physics is more complicated than semiconductor surface physics. The importance in Silicon technology, the semiconductor/insulator (Si/TiO_2) interface and defects on its neighbourhood have been extensively studied in the past four decades. In general, there are several possible sources of error, which cause deviations from the ideal MOS behaviour such as electrical properties, must be taken into account. The study of *I-V* and *C-V* characteristics obtained at room temperature does not provide the detailed information about the charge transport process at the Si/TiO_2 interface. The temperature dependent electrical characteristics provide the information regarding the charge transport process through MOS contacts and also give a better picture of the conduction mechanisms [12]. The leakage current density of TiO_2 thin films can be further reduced by annealing in various gas environments such as O_2, N_2O and N_2, among these the common annealing process was in air ambience because it improves the structural order, dielectric constant and the reduction of defect states. This paper deals with the TiO_2 thin film deposition and annealing studies [13]. Due to the presence of oxide layer (TiO_2/SiO_2) and two region of interfaces metal/oxide and silicon/oxide have been extensively studied in the past four decades. The epitaxial growth of TiO_2 thin films deposited by Pulsed laser ablation, further improved the thin films as MOS Ni/*n*-TiO_2/*p*-Si for rectifying contact [14].The MOS structures of Pt/TiO_2/Si present that the dielectric constant of the TiO_2 thin film deposited between the Silicon substrate and platinum electrode. The growth of the interfacial layer seems to be reduction of oxygen vacancies. The MOS device different appearance as compared to the ideal case due to the presence of interface trapped density, effective oxide charge density and localized interface states. Then the leakage current mechanism in MOS (Pt/TiO_2/Si) structures capacitor at high electric field and at high temperature is due to Schottky emission.

2. Experimental

The TiO_2 thin films were prepared by spray pyrolysis technique under optimum conditions using Titanium (IV) Isopropoxide as a source material, Acetyl Acetonate as a complexing agent and Absolute ethanol as solvent. Before deposition, the silicon (100) wafers were cleaned using RCA-1 and RCA-2 [15]. TiO_2 thin films were deposited at a substrate temperature of 350 °C using 0.1 mol TiO_2 precursor solution. After deposition, isochronal annealing studies were carried out at various temperatures of 400, 500 and 600 °C for constant time of 30 min under air ambient. Electrical studies were made

by analyzing *C-V* and *I-V* characteristics of the deposited films. The electrical contacts were made by depositing platinum via a shadow mask on the surface of the TiO_2 layer using sputtering technique. The area of the dot diameter 7.5×10^{-4} cm^2. Other hand the back contact were made aluminum layer deposited of the silicon (100) wafer using thermal evaporation technique (Hindhivac vacuum coating unit Model 15F6). The devices were electrically characterized by Agilent Technologies B1500A Semiconductor device analyzer for both *I-V* and *C-V* studies. The bias was applied to the back contact (Si substrate) while the top contact was kept at the ground potential. Positive and negative bias sweeps were applied across zero bias. This paper presents the study of *I-V*, *C-V* and C^{-2}-*V* (hysteresis loop) characteristics of MOS (Pt/TiO_2/Si) device were made and estimate the electrical properties.

3. Result and Discussion

3.1. I-V Characteristics

Fig. 1 shows the measured forward and reverse bias Current density-Voltage characteristics of the fabricated MOS (Pt/TiO_2/*p*-Si) capacitor using as deposited at 300 °C and annealed TiO_2 thin films at 400, 500 and 600 °C. The applied voltage was varied from –1 V to +1 V, these devices are presented rectifying behaviour. Ideality factor *n* (*I-V*) for the MOS capacitor was obtained from the linear region of the forward characteristics ln (*I*) versus voltage using equation [16]. Where *k* is the Boltzman constant, *T* is the temperature and *q* is the electronic charge:

$$n=\frac{q}{kT}\left(\frac{dV}{d\ln I}\right). \quad (1)$$

Various electrical parameters such as ideality factor (*n*), barrier height (Φ_B), saturation current (I_0), leakage current (I_C), series resistance (R_C) were calculated and estimated values are tabulated in Table 1. It can be observed that the decrease in ideality factor with increase in heat treatment may be attributed to the potential drop across the interfacial insulating layer of TiO_2 at the metal/semiconductor interface. The values of the saturation current were calculated by extrapolating the linear region to the ordinate and estimated as shown in the Table 1. The large value of the leakage current density (at –1 V) decrease with increase in annealing temperature, which may be attributed to the fabrication

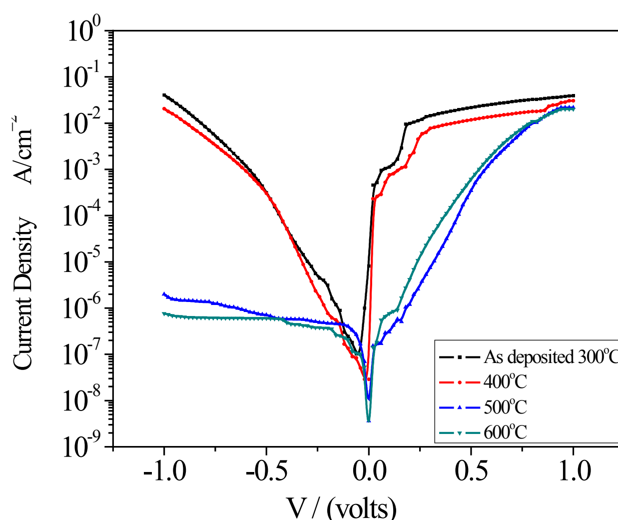

Fig. 1. Current–Voltage characteristics of Pt/TiO_2/Si for as deposited and annealed at different temperatures

Table 1. Electrical parameters of Pt/TiO_2/Si (MOS) structure from Current–Voltage

Sample	As deposited 300 °C	Annealing 400 °C	Annealing 500 °C	Annealing 600 °C
$n_{(FB\ I-V)}$	3.014	2.78	2.64	2.24
Jc, A/cm^2 at 1 V	$1.19\cdot10^{-4}$	$9.14\cdot10^{-5}$	$7.4\cdot10^{-5}$	$4.2\cdot10^{-5}$
$\Phi_{B(FB\ I-V)}$, eV	0.7004	0.7146	0.82879	0.840402
I_o, A	$5.89\cdot10^{-9}$	$1.02\cdot10^{-8}$	$7.15\cdot10^{-11}$	$4.56\cdot10^{-11}$
$n_{(dV/d\ln(I))}$	2.78	2.27	2.2	2.054
$\Phi_{B(H(I))}$	0.65	0.75	0.829	0.862
$R_{C\ (dV/d\ln(I))}$, Ω	129.59	139.5	168.109	194.102
$R_{C\ (H(I))}$, Ω	116.96	176.34	182.2	208,5

method and generation of the defects in the interface between silicon/TiO_2 and high series resistance of as deposited TiO_2 thin films and also the top electrode Pt acts as higher conductivity [17]. The barrier height is calculated from equation, where A^* is the effective Richardson constant (32 A/cm^{2}K^2) for *p*-type silicon, A is the area of the device (1.96e^{-3}cm^2), *T* is the room temperature (300 K), *q* is the electronic charge, *k* is the Boltzmann constant:

$$\Phi_{B0} = \left(\frac{KT}{q}\right)\ln\left(\frac{AA^*T^2}{I_0}\right). \quad (2)$$

The estimated values are tabulated in Table 1 and it is observed that the barrier height increases with increasing annealing temperature this may be due to immobilized radical are present in the metal/insulating layer interfaces. And also further analysed method developed by Cheung and Cheung's functions are given as [18,19]:

$$\frac{dV}{d\ln I} = IR_S + n\left(\frac{kT}{q}\right), \quad (3)$$

$$H(I) = n\Phi_B + IR_S = V - \frac{nkT}{q}\ln\left(\frac{I}{AA^*T^2}\right). \quad (4)$$

where *V* is voltage; R_S is series resistance; Φ_B is barrier height

Figs. 2 and 3 show the plots of d*V*/d(ln*I*) versus *I* and *H*(*I*) versus *I* corresponding to Cheung functions of below equations extracted from experimental forward *I-V* characteristics data. In Fig. 2 the obtained slope gives the series resistance, while the intercept on *y*-axis is the ideality factor which is nearer to those obtained from the ln(*I*)-*V* plot. The series resistance (R_S) plays a crucial role in the forward *I-V* characteristics of the MOS structure at higher applied voltage. Thus, Fig. 3 also gives the straight line with current axis intercept equal to the barrier height. The slope of this straight line provides the series resistance (R_s), which can be used to check the consistency of this approach. The estimated values of *n*, Φ_B and (R_s) from Cheung functions are tabulated in table 1, which are close to those obtained from *I-V* forward region. The series resistance (*Rs*) was found to increase with increase in temperature, this may be due to increased effective oxide thickness of TiO_2 film with increased annealing temperature.

3.1. C-V Characteristics

Fig 4. presented the *C-V* characteristics of MOS (Pt/TiO_2/Si) devices, the voltage sweep from –1 V to +1 V at 1 MHz and its shows accumulation, inversion and depletion regions. It is observed that a strong accumulation is observed with high value of capacitance for the device annealed at 600 °C, which is attributed to the variation of the interface states density and dangling bonds which are associated with silicon/Oxide and metal/oxide interface. The capacitance becomes up and down in inversion and accumulation region as gate voltage

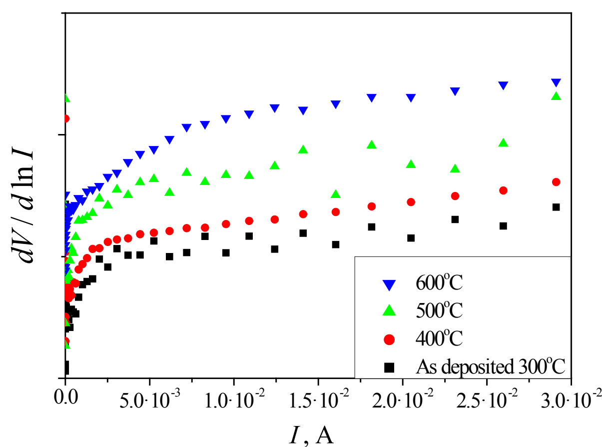

Fig. 2. dV/dln(I)-I characteristics of Pt/TiO_2/Si for as deposited and annealed at different temperatures

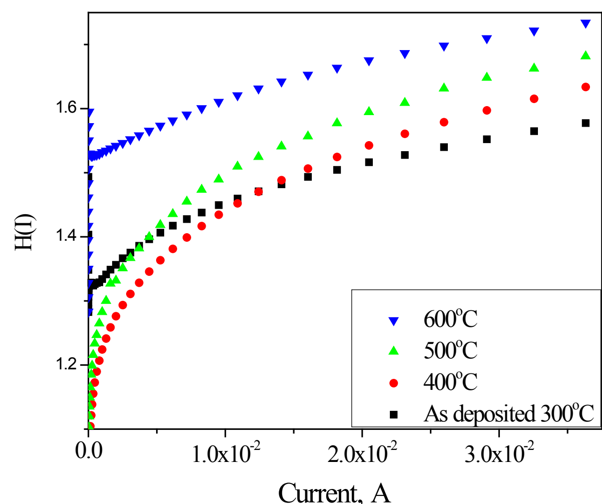

Fig. 3. H(I)-I characteristics of Pt/TiO_2/Si for as deposited and annealed at different temperatures

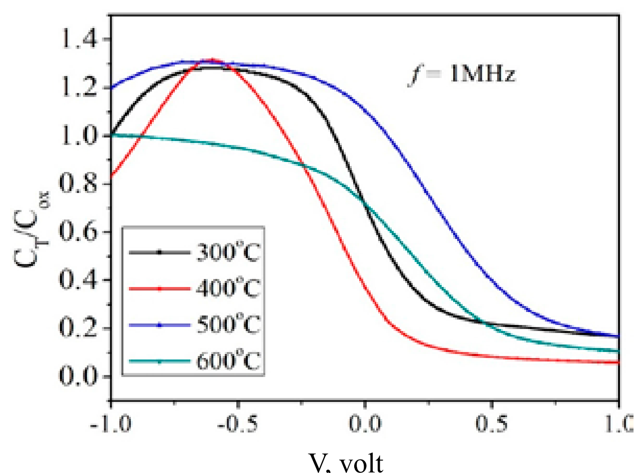

Fig. 4. *C-V* characteristics of Pt/TiO_2/Si for as deposited and different annealing temperature

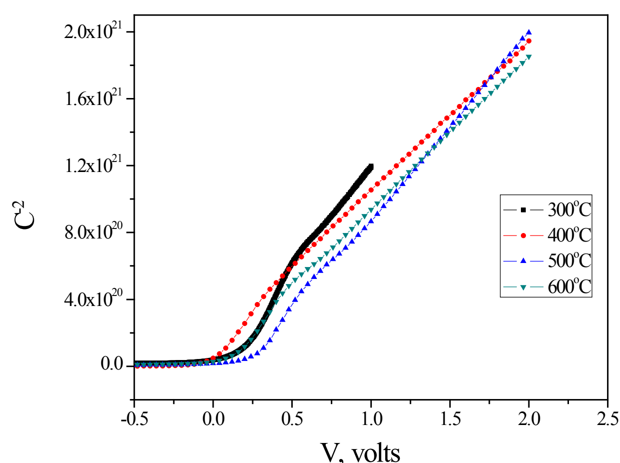

Fig. 5. C^{-2}-V characteristics of Pt/TiO_2/Si for as deposited and annealed at different temperatures

increase, which is attributed due to higher leakage current in TiO_2/Si interface. The slope estimated from the C^{-2}-V plot (Fig. 5) of device is substituted in below equation, which gives the oxide charge concentration as tabulated in Table 2:

$$\left(\frac{dC^{-2}}{dV}\right)=\left(\frac{2}{\varepsilon_s q A^2 N_D}\right), \quad (5)$$

where ε_s dielectric constant of semiconductor (silicon) $\varepsilon_s = 11.8\varepsilon_0$ (ε_0 is $8.85\cdot10^{-14}$ F/cm), A is area and q is charge, N_D is doping concentration.. It can be observed from the C^{-2}-V plot that the intercept on voltage axis gives the flat band voltage and are tabulated in Table 2. The increasing temperature of films under air ambient which leads to increase in oxygen vacancies and acceptor trap density which leads to the flat band voltage shifts towards positive. It can be seen that the oxide charge concentration at 400 °C with the annealing temperature, which may be due to the reduction of the interface trapped charges as seen in Table 2. It appears that drastic variation of Capacitance (C_{ox}) per unit area at 400 °C, this attributed that, between silicon/oxide interface the impurity concentration randomly variation takes place. And also the most interface trap density neutralised at this particular temperature. The similar study of MOS in *C-V* plot reported [20, 21]. The *C-V* hysteresis loop of MOS devise measured in counter clockwise at frequency of 1 MHz for different annealing temperatures is shown in Fig. 6. Presents *C-V* hysteresis loop the dc voltage swept sufficiently slowly to allow the inversion charge to form but the ac probe frequency is too high for the inversion charge to be able to responds, then high frequency curve is

Таблица 2. Электрические параметры структуры Pt/TiO_2/Si (МОП) по данным ВФХ

Sample	As deposited at 300 °C	Annealed at 400 °C	Annealed at 500 °C	Annealed at 600 °C
$C_{ox}\cdot10^{-7}$, f/cm^2	1.195	8.16	2.05	1.68
V_{FB}, B	−0.0705	−0.2148	−0.225	0.00992
∇V_{FB}, , V	0.0466	0.07372	0.13766	0.0089
ΔC, f	$2.23\cdot10^{-9}$	$4.19\cdot10^{-9}$	$1.01\cdot10^{-8}$	$1.01\cdot10^{-12}$
D_{it}, cm^{-1}eV^{-1}	$1.36\cdot10^{10}$	$2.54\cdot10^{10}$	$6.30\cdot10^{10}$	$6.3\cdot10^{6}$
N_{eff}, cm^{-3}	$8.02\cdot10^{11}$	$6.07\cdot10^{12}$	$1.23\cdot10^{12}$	$1.19\cdot10^{12}$
Q_{OT}, f/cm^2	$3.71\cdot10^{11}$	$1.76\cdot10^{11}$	$3.46\cdot10^{10}$	$9.37\cdot10^{09}$
N_{ox}, cm^{-3}	$2.34\cdot10^{15}$	$2.85\cdot10^{15}$	$3.15\cdot10^{15}$	$3.32\cdot10^{15}$

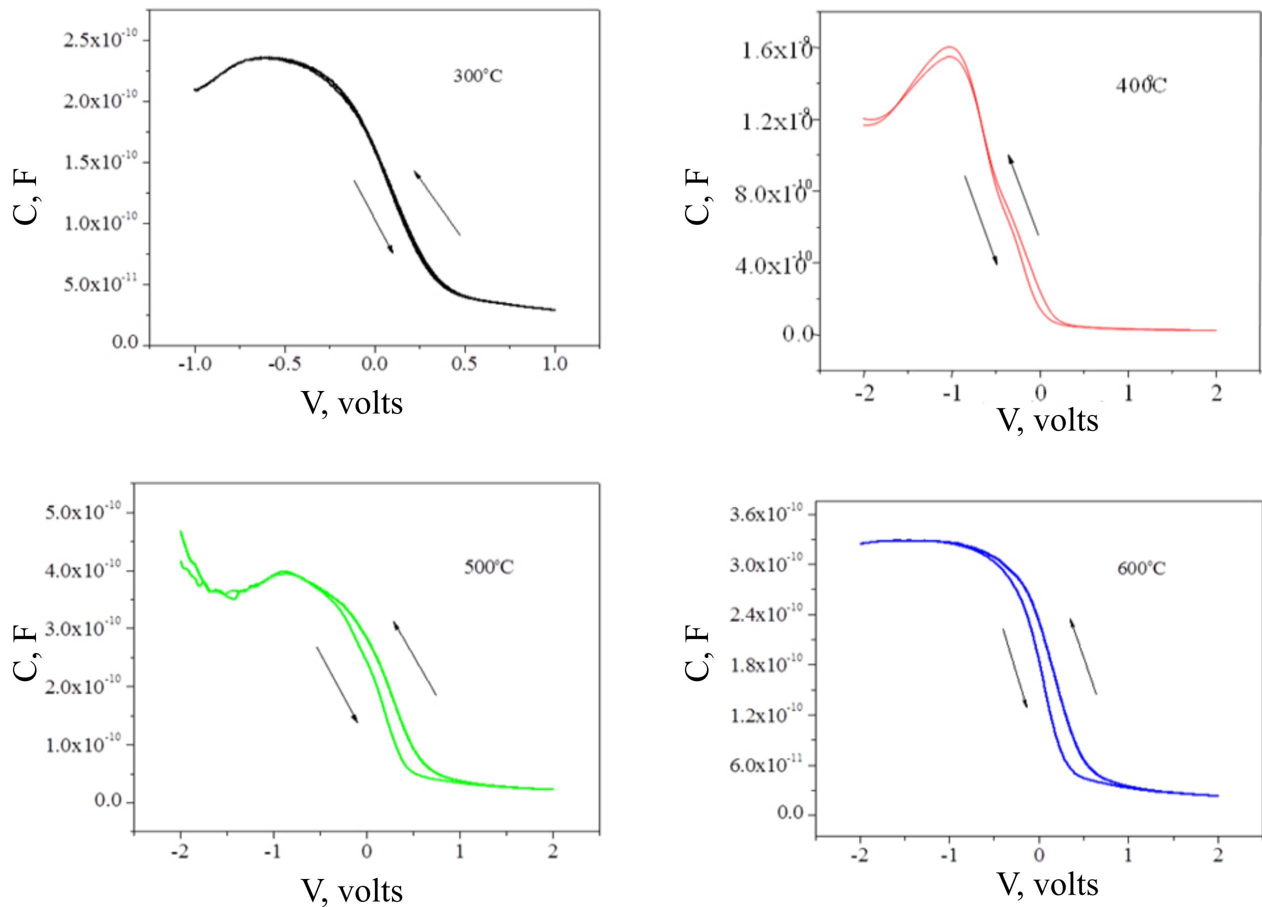

Fig. 6. *C-V* hysteresis loop of Pt/TiO_2/Si for as deposited and annealed at different temperatures

obtained. The hysteresis loop found to improve for all bias modes of accumulation, depletion and inversion as a function of heat treatment, which may be attributed to the decrease in leakage current and reduction of the interface trap density. In the *C-V* hysteresis, the voltage sweep in counter clock wise direction (–1 V to +1 V to –1 V) does not trace the same path as that of clock wise and shifted to lower voltages due to effective charge densities present in the interface between metal and silicon. The strong bias mode loop was observed at annealing temperature of 600 °C which may be due to lower value of interface trapped charge i.e., $6.3 \cdot 10^6$ cm^{-1}eV^{-1} and reduction in the dangling bonds [22, 23]. Interface trap density, it is defined as the dangling bands at the surface of a semiconductor are responsible for distributed energy level called surface states or interface states density within the forbidden gap at the surface of the semiconductor, which is calculated using *C-V* characteristics in following relation [24]:

$$D_{\text{it}} = \frac{dC}{q}\left(1 - \frac{C_{HF} + \Delta C}{C_{\text{ox}}}\right)\left(1 - \frac{C_{HF}}{C_{\text{ox}}}\right), \qquad (6)$$

where $\Delta C = C_{HF} - C_{LF}$, C_{LF} and C_{HF} *are* lower frequency region (lesser than the 1 KHz) and higher frequency region (greater than 1 MHz), C_{ox} is the Capacitance per unit area from and q is charge ($1.69 \cdot 10^{-19}$ C). The interface trap density D_{it} values are tabulated in Table 2 and values are found to be lower as compared to SiO_2. During annealing, the TiO_2 thin films gets oxidized which leads to the variation in dangling bonds. It is also observed that, annealing at 600 °C, the interface trapped density of TiO_2 thin films suddenly reduced by 4 order of magnitude ($6.3 \cdot 10^6$ cm^{-1}eV^{-1}) as compared to those of lower temperature annealed films. This may be due to the increased crystallinity of the TiO_2 thin films and reduced leakage current ($4.2 \cdot 10^{-5}$A). The

effective charge density (N_{eff}) is related to fixed oxide charge (Q_F), mobile ionic charge (Q_M) and oxide trapped charge (Q_{OT}) as in equation:

$$N_{eff} = \frac{Q_F + Q_M + Q_{OT}}{q}. \quad (7)$$

For the calculation of the effective oxide charge density, the expression by Nicollian and Brews [25]. It was found that the N_{EEF} was related to metal (Platinum) - Semiconductor junction and flat band voltage by,

$$N_{eff} = \frac{C_{ox}(\varphi_{MS} - V_{FB})}{Aq}, \quad (8)$$

where A is the area, C_{ox} is the capacitance per unit area and q is charge of an electron ($1.69 \cdot 10^{-19}$ C), V_{FB} is the flat band voltage and φ_{MS} is the metal semiconductor work function difference. The estimated values of N_{eff} are tabulated in Table 2 and it is found to decrease with annealing temperature, which is attributed to the increase in leakage current upon electrical stress. This suggests that near interface states creates neutral trapped charges in insulating layer. The oxide trapped charges are not located at the silicon/oxide interface but are distributed throughout oxide. The distribution of Q_{OT} must be known for proper interpretation of C–V curves. These are not introduced during the device fabrication, but in C-V characteristics during the gate voltage sweeping process electron or holes can be injected from gate or substrates. The oxide trapped charge distribution in oxide was estimated using the equation [26]:

$$Q_{OT} = \left(\frac{C_{ox} \nabla V_{FB})}{q}\right), \quad (9)$$

where ∇V_{FB} are flat band voltage shifts, C_{ox} is the Capacitance per unit area from and q is charge ($1.69 \cdot 10^{-19}$ C). The value of Q_{OT} tabulated in Table 2. These values are found to decrease with increase in heat treatment which may be attributed to the ionizing radiation, avalanche injection, Schottky emission, Fowler–Nordheim tunneling, or other mechanisms.

4. Conclusion

It is found that interfacial layer has crucial effect on electrical properties role MOS structures of Pt/TiO_2/Si. From I-V characteristics estimated parameter such as ideality factor (n) and barrier height (Φ_B) were found to be comparable as estimated from the model using Cheung functions. The estimated values of the barrier height increases with increasing annealing temperature, this may be potential drop across the interfacial insulating layer of TiO_2 at the metal/semiconductor interface. The series resistance (Rs) of device found to increase with increase in heat treatment. The observed decrease in leakage current with annealing temperature was attributed to the decrease in dangling bonds. From C-V characteristics, the oxide charge concentration (N_{ox}), flat band voltage (V_{FB}), interface trap density (D_{it}) and effective charge density (N_{eff}) were estimated. These values were found to decrease with the annealing temperature, due to the reconstruction and rearrangement of Ti and O atoms. From C-V hysteresis loop, in the counter clock wise direction, it is observed that hysteresis shifted to lower voltages due to effective charge densities present in the MOS structure and the strong accumulation region was obtained for higher temperature annealed TiO_2 film may be due to the reduction of interface trapped charge and oxide trapped charge density.

Contribution of the authors

The authors contributed equally to this article.

Conflict of interests

The authors declare that they have no known competing financial interests or personal relationships that could have influenced the work reported in this paper.

Reference

1. Nakaruk A., Ragazzon D., Sorrel C. C. Anatase–rutile transformation through high-temperature annealing of titania films produced by ultrasonic spray pyrolysis. *Thin Solid Films*. 2010;518(14): 3735–3742. https://doi.org/10.1016/j.tsf.2009.10.109

2. Li W., Ni C., Lin H., Huang C. P., Ismat Shah S. Size dependence of thermal stability of TiO_2 nanoparticles. *Journal of Applied Physics*. 2004;96(11): 6663–6668. https://doi.org/10.1063/1.1807520

3. Murad E. Raman and X-ray diffraction data on anatase in fired kaolins. *Clays and Clay Minerals*.2003;51(6); 689–692. https://doi.org/10.1346/cmn.203.0510611

4. Rausch N., Burte E. P. Thin TiO_2 films prepared by low pressure chemical vapor deposition. *Journal of*

The Electrochemical Society. 1993;140(1): 145–149. https://doi.org/10.1149/1.2056076

5. Kemell M., Pore V., Ritala M., Leskelä M., LindénM. Atomic layer deposition in nanometer-level replication of cellulosic substances and preparation of photocatalytic TiO_2/cellulose composites. *Journal of the American Chemical Society*. 2005;127(41): 14178–14179. https://doi.org/10.1021/ja0532887

6. Kim D. J., Hahn S. H., Oh S. H., Kim E. J. Influence of calcination temperature on structural and optical properties of TiO_2 thin films prepared by sol–gel dip coating. *Materials Letters*. 2002;57(2): 355–360. https://doi.org/10.1016/s0167-577x(02)00790-5

7. Suda Y., Kawasaki H., Ueda T., Ohshima T. Preparation of high quality nitrogen doped TiO_2 thin film as a photocatalyst using a pulsed laser deposition method. *Thin Solid Films*. 2004;453–454: 162–166. https://doi.org/10.1016/j.tsf.2003.11.185

8. Wang H., Chen L., Wang J., Sun Q., Zhao Y. A micro oxygen sensor based on a nano sol-gel TiO_2 thin film. *Sensors*. 2014;14(9): 16423–16433. https://doi.org/10.3390/s140916423

9. Kikuchi H., Kitano M., Takeuchi M., Matsuoka M., Anpo M., Kamat P. V. Extending the photoresponse of TiO_2 to the visible light region: photoelectrochemical behavior of TiO_2 thin films prepared by the radio frequency magnetron sputtering deposition method. *The Journal of Physical Chemistry B*. 2006;110(11): 5537–5541. https://doi.org/10.1021/jp058262g

10. Chandrashekara H. D., Angadi B., Shashidhar R., Murthy L. C. S., Poornima P. Optical properties of pseudo binary oxides $(TiO_2)_{1-x}$-$(Al_2O_3)_x$ thin films prepared by spray pyrolysis technique. *Materials Today: Proceedings*. 2006;3(6): 2027–2034. https://doi.org/10.1016/j.matpr.2016.04.105

11. Khan M. I., Imran S., Shahnawaz Saleem M., Ur Rehman S. Annealing effect on the structural, morphological and electrical properties of TiO_2/ZnO bilayer thin films. *Results in Physics*. 2018;8: 249–252. https://doi.org/10.1016/j.rinp.2017.12.030

12. Ramana C., Becker U., Shutthanandan V., Julien C. Oxidation and metal-insertion in molybdenite surfaces: evaluation of charge-transfer mechanisms and dynamics. *Geochemical Transactions*. 2008;9(1). https://doi.org/10.1186/1467-4866-9-8

13. Chandrashekara H. D., Angadi B., Shashidhar R., Murthy L. C. S., Poornima P. (2016). Isochronal effect of optical studies of TiO_2 thin films deposited by spray pyrolysis technique. *Advanced Science Letters*.2016; 22(4): 739–744. https://doi.org/10.1166/asl.2016.6975

14. Kumar A., Sharma K. K., Chand S., Kumar A. Investigation of barrier inhomogeneities in I-V and C-V characteristics of Ni/n-TiO_2/*p*-Si/Al heterostructure in wide temperature range. *Superlattices and Microstructures*. 2018;122: 304–315. https://doi.org/10.1016/j.spmi.2018.07.034

15. Kern W. *Hand book of semiconductor cleaning technology*. Noyes Publications; 1993. 623 p.

16. Sze S. M. *Physics of semiconductor devices*. New York: John Wiley and Sons*;* 1981. 868 p.

17. Gümüş A., Türüt A., Yalçin N. Temperature dependent barrier characteristics of CrNiCo alloy Schottky contacts on n-type molecular-beam epitaxy GaAs. *Journal of Applied Physics*. 2002;91(1): 245–250. https://doi.org/10.1063/1.1424054

18. Pakma O., Serin N., Serin T., Altındal Ş. The effects of preparation temperature on the main electrical parameters of Al/TiO_2/*p*-Si (MIS) structures by using sol–gel method. Journal of Sol-Gel Science and Technology. 2009;50(1): 28–34. https://doi.org/10.1007/s10971-009-1895-4

19. Yen C.-F., Lee M.-K. Low equivalent oxide thickness of TiO_2/GaAs MOS capacitor. *Solid-State Electronics*. 2012;73: 56–59. https://doi.org/10.1016/j.sse.2012.03.007

20. Rathee D., Kumar M., Arya S. K. (2012). Deposition of nanocrystalline thin TiO_2 films for MOS capacitors using Sol–Gel spin method with Pt and Al top electrodes. *Solid-State Electronics*. 2012;76: 71–76. https://doi.org/10.1016/j.sse.2012.04.041

21. Wei D., Hossain T., Garces N. Y., ... Edgar J. H. Influence of atomic layer deposition temperatures on TiO_2/*n*-Si MOS capacitor. *ECS Journal of Solid State Science and Technology*. 2013;2(5): N110–N114. https://doi.org/10.1149/2.010305jss

22. Chiu H.-C., Lin C.-K., Lin C.-W., Lai C.-S. Investigation of surface pretreatments on GaAs and memory characteristics of MOS capacitors embedded with Au nano-particles. *Microelectronics Reliability*. 2012;52(11): 2592–2596. https://doi.org/10.1016/j.microrel.2012.05.002

23. Murray H., Martin P. A unified channel charges expression for analytic MOSFET modeling. *Active and Passive Electronic Components*. 2012; 1–12. https://doi.org/10.1155/2012/652478

24. Yen C.-F., Lee M.-K. Low equivalent oxide thickness of TiO_2/GaAs MOS capacitor. *Solid-State Electronics*. 2012;73: 56–59. https://doi.org/10.1016/j.sse.2012.03.007

25 Nicollian E. H, Brews J. R. *MOS (Metal Oxide Semiconductor) physics and pechnology*. John Wiley & Sons; 1982. 928 p.

26. Schroder D. K. *Semiconductor material and device characterization*. John Wiley & Sons; 2006. 800 p.

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