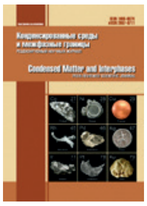

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TiO_2 thin-film dielectric properties are impacted by annealing

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Abstract

Purpose: This study investigates the structural, morphological, and dielectric properties of TiO_2 thin films deposited using the Spray Pyrolysis Deposition (SPD) process and annealed at various temperatures.

Experimental: X-ray diffraction (XRD) analysis confirms the absence of an amorphous phase at 300 °C, while the anatase and rutile phases emerge at 400 °C, 500 °C, and 600 °C, with crystallite sizes increasing from 10.62 to 17.35 nm. Scanning electron microscopy (SEM) reveals a consistent grain growth trend, with grain sizes exceeding XRD estimates. Energy-dispersive X-ray (EDAX) spectroscopy confirms a stoichiometric Ti:O ratio and uniform nanoparticle distribution. The dielectric properties of Pt/TiO_2/Si MOS capacitors were analyzed, demonstrating improved electrical stability with annealing. Conductance studies indicate a reduction in defect states, enhanced crystallinity, and stable dielectric behavior at higher frequencies. The hysteresis loop analysis reveals decreased losses at 600 °C due to minimized trapped charges and broken bonds. Impedance spectroscopy highlights capacitive behavior, with relaxation peaks at 400 °C, 500 °C, and 600°C, while conductance measurements indicate thermal activation of charge carriers.

Conclusions: These findings suggest that TiO_2 thin films exhibit promising dielectric properties for potential applications in Si-based MOS capacitors and VLSI technology.

Keywords: Loss tangent, Angular frequency, Conductance, Series resistance, Impedance

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1. Introduction

The heat treatment procedure known as annealing has a substantial effect on the dielectric properties of thin films of titanium dioxide (TiO_2) The TiO_2 is a material that is frequently used in electronic devices because of its excellent optical transparency, chemical stability, and dielectric constant. These devices include sensors, memory devices, and capacitors. The substantial number of studies published in the literature over the past ten years indicates the interest in TiO_2 [1-9]. TiO_2 thin-film production using atomic layer deposition and its dielectric characteristics [10]. TiO_2 thin films produced by pulsed laser deposition: their structural and dielectric characteristics [11]. Spray pyrolysis is the most used method of film synthesis of all the approaches [12]. Technology-related applications for titanium oxide films include solar cells, thin-film transistors, sensors, and other devices. Numerous techniques, including thermal evaporation of oxide powders, electron beam evaporation, chemical vapor deposition, sputtering, sol–gel, and spray deposition, can be used to generate TiO_2 thin films. However, each technique has pros and cons. Since spray deposition offers low processing temperatures, low cost of manufacturing, and improved control over the deposition settings, it affords an easy solution to include TiO_2 devices into Si technology. In order to improve device performance, future nanoelectronic devices may use metal oxides with high dielectric constants in place of TiO_2 in the gate and high-mobility semiconductors like Si in the active channel [13, 14]. Critical performance parameters of MOS capacitors and transistors for aggressive oxide scaling with equivalent oxide thickness (EOT) are determined by the interface between dielectric materials and Si. The capacitance methods of semiconductor examination, which provide comprehensive information about the properties of localized electronic states (or energy levels), have gained significant recognition [15–17]. After being annealed in an oxygen environment, the TiO_2 thin films' dielectric constant greatly increased. Improvements in the films' crystallinity and decrease in oxygen vacancies are responsible for this increase in the dielectric constant. These films can be used in capacitors, transistor gate dielectrics, and other electronic devices because of their enhanced dielectric qualities [18]. "Surface states" refers to the localized electronic states that are connected to the surface area. Their existence is caused by the periodic lattice structure breaking at the surface, surface preparation, oxide layer development, and semiconductor impurity concentration. The existence of an interfacial layer between the contact materials and interface states at the oxide layer/semiconductor interface, however, frequently disturbs this idealized scenario. In this study, the dielectric parameters for (Pt/TiO_2/Si) MOS capacitors in the voltage range of -2V to +2V at different temperatures were examined. The dielectric parameters were obtained from *C*–*V*, tan(δ)–Voltage, G/ω–ω, and *Z*–*f* measurements. The capacitors were deposited at 300 °C and then annealed at 400 °C, 500 °C, and 600 °C.

The primary goal of this research involves growing. Depending on the annealing temperature, annealing usually improves the films crystalline structure by converting their amorphous or less crystalline structures into clearly defined crystalline phases like rutile or anatase. Because there are fewer flaws and grain boundaries in the film as a result of this increased crystalline, the dielectric qualities—such as a higher dielectric constant and less dielectric loss-are improved.

2. Experimental

Acetyl acetonate was used as a complexing agent, absolute ethanol was used as a solvent, and titanium (IV) isopropoxide was used as the source material for the spray pyrolysis deposition (SPD), which produced the TiO_2 thin films under ideal conditions [19]. The silicon wafers were cleaned using RCA-1 and RCA-2 prior to deposition. TiO_2 thin films were deposited using 0.1 mol TiO_2 precursor solution at 300 °C substrate temperature. Following deposition, isochronal annealing experiments were conducted in air at 400 °C, 500 °C, and 600 ºC for a continuous duration of 30 minutes.

An EDAX and SEM were used to study the surface morphology under a field emission scanning electron microscope (ULTRA 55, Karl Zeiss). To investigate the dielectric characteristics, 100 platinum dots were deposited to create electrical connections. The microstructure, surface morphology, and general quality of the TiO_2 thin films are similarly impacted by annealing. It can boost the density of the film and lessen the existence of residual stresses, both of which add to the improved dielectric performance. Because of this, annealed TiO_2 thin films have better electrical insulation and stability, which makes them more appropriate for use in optoelectronic and electronic devices.

2.1. Material characterization

The X-ray diffraction (XRD) patterns of TiO_2 films as-deposited at 300 °C and those annealed in air at 400 °C, 500 °C, and 600 °C are displayed in Fig. 1. There are no noticeable peaks in the amorphous structure of the film as it was deposited at 300 °C. The anatase phase of TiO_2 is shown by peaks in the film that was annealed at 400 °C. Along with the anatase phase, the films annealed at 500 °C and 600 °C exhibit the appearance of peaks corresponding to the rutile phase of TiO_2. Higher annealing temperatures result in more intense rutile peaks, suggesting a larger percentage of the rutile phase at higher temperatures [20].

A distinct pattern of growing crystallite size with increasing annealing temperature is seen in the estimated crystallite sizes of 10.62, 13.73, 16.04, and 17.35 nm derived from X-ray diffraction using the Scherrer formula. Grain sizes derived from SEM pictures are, on average, 13.6, 16.3, 17.5, and 27.3 nm. As expected given that grains seen in SEM may include several crystallites, the grain sizes derived from SEM are consistently greater than the crystallite sizes ascertained via XRD. This disparity raises the possibility of smaller crystallites coalescing at higher temperatures as well as the presence of contributions from grain boundaries. Smooth surface roughness and a consistent, compact distribution of grains are shown in the SEM picture of the deposited TiO_2 films in Fig. 2a. The histograms revels that, the *x*-axis represents grain size ranges, and the *y*-axis shows the number of grains in each size range. Temperature affects the distribution of grain sizes. The distribution of grain sizes in TiO_2 films at various temperatures is revealed by the investigation. The histograms demonstrate that the distribution of grain sizes changes with temperature, with smaller grain clusters becoming more pronounced at 500 °C and 600 °C, expanding at 400 °C, and more densely packed at 300 °C.

The energy dispersive analysis X-ray spectrum is displayed in Fig. 2b. As samples are deposited and annealed, the weight fraction of oxygen and Ti changes. The produced TiO_2 thin films' chemical composition analysis shows good stoichiometry. The weight % of Ti and oxygen fluctuates for samples that are annealed and deposited, according to energy dispersive analysis X-ray spectrum analysis. The results obtained are in good agreement with the previously reported works [21, 22].

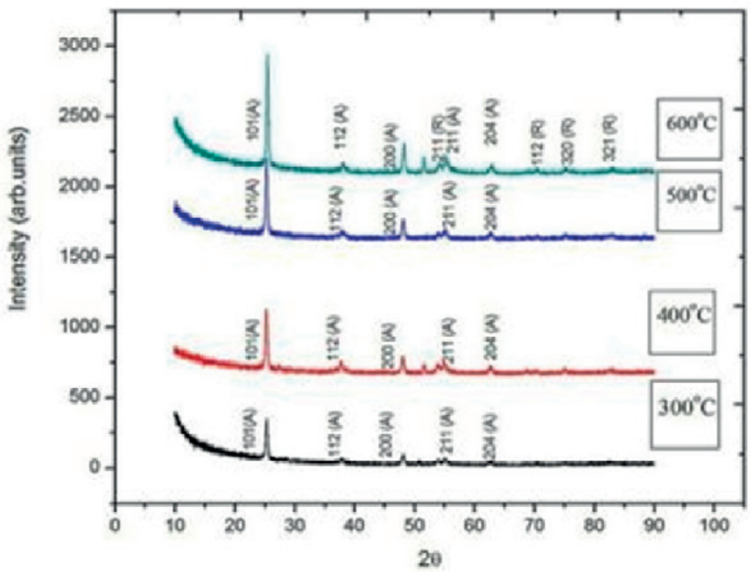
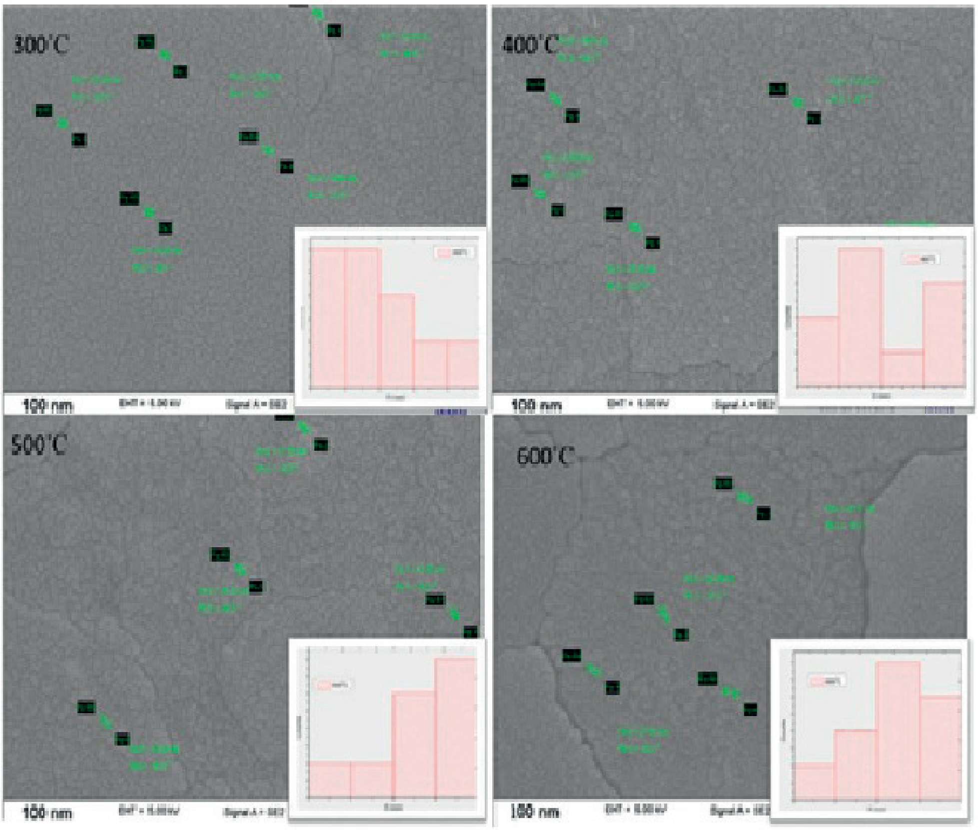
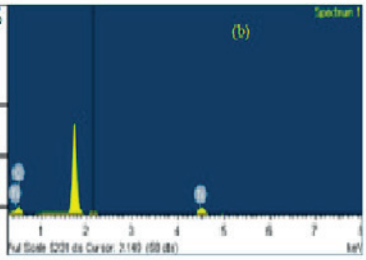


Fig. 1. XRD pattern of air-annealed and as-deposited thin films of TiO_2



a



Element	Weight%	Atomic%
OK	63.42	83.85
TiK	36.58	16.15
Totals	100.00	

b

Fig. 2. (a) SEM (inset: Histogram) and (b) EDX spectrum of TiO$_2$ thin films as deposited

2.2. Dielectric features

The tan(δ)–Voltage characteristics for both deposited and annealed films are displayed in Fig. 3 as a function of voltage (+2V to –2V) at a constant frequency of 1MHz. Near zero bias, a tiny peak emerges, which could be the result of the flat band shift making the dielectric losses more noticeable. As heat treatment is applied, it can be seen that the resulting dissipation factor or loss factor decreases, which reduces interface trapped charge and dangling bonds. Low-frequency impedance is controlled by the interface states with the substrate and the dielectric properties of the TiO$_2$ layer, as shown in Fig. 4. Capacitive reactance decreases with frequency, allowing the intrinsic characteristics of the dielectric material to have a greater impact on impedance behavior. An injection locking phenomena involving oxide charge density oscillation may be the cause of the lowering impedance values with increasing frequency [23, 24]. The dielectric and conductive characteristics of the films are revealed by conducting conductance versus angular frequency analysis for MOS devices with as-deposited TiO$_2$ thin films annealed at different temperatures [25]. Interface states with the substrate and the dielectric characteristics of the TiO$_2$ layer control low-frequency impedance. Because capacitive reactance decreases with frequency, the inherent

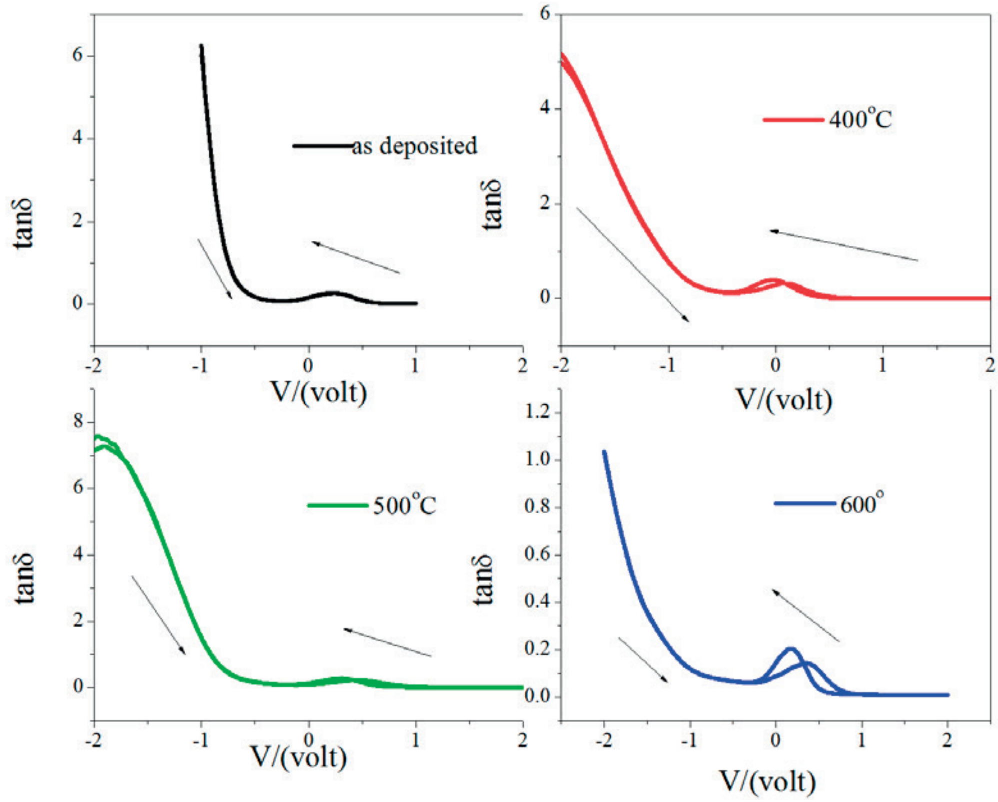


Fig. 3. tan δ-Voltage characteristic of MOS devices for TiO2 thin films annealed at various temperatures

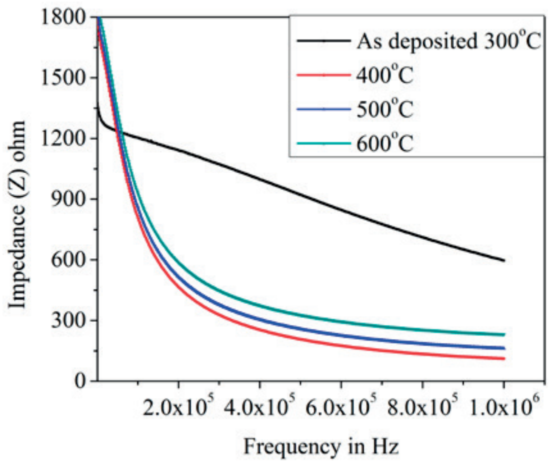


Fig. 4. Impedance versus frequency of MOS devices for TiO$_2$ thin films annealed at various temperatures

properties of the dielectric material can have a greater impact on impedance behavior. The decreasing impedance values at increasing frequencies could be explained by an injection locking phenomenon involving oxide charge density oscillation.

The intriguing characteristic is that conductance increases with frequency shown in Fig. 5, this may be due to an interface-trapped charge [26]. An increasing annealing temperature is shown to cause a decrease in conductance, which is ascribed to an increase in leakage current [27]. The variation of dielectric losses with applied voltage is shown by the tan(δ) – Voltage characteristic of MOS devices employing as-deposited TiO$_2$ thin films. Due to dielectric property changes, this characteristic can be significantly altered when TiO$_2$ thin films are annealed at different temperatures. The tan(δ) becomes more stable at higher annealing temperatures across a wider voltage range. This stability suggests lower leakage currents and better film quality. The Fig. 6 shows parallel resistance (R_p) versus frequency at different temperatures for a MOS device. The steepest decrease is at lower frequencies, while higher frequencies show more gradual decreases. The device's AC response characteristics and temperature dependence suggest thermal activation of charge carriers, and the variation in resistance patterns suggests changes in the material's electronic properties. The MOS device's series resistance (R_s) is displayed against

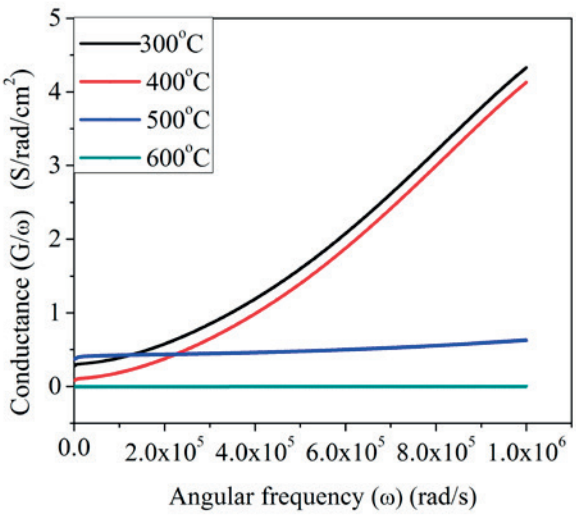


Fig. 5. (*G*/ω-ω) conductance versus angular frequency of MOS devices for TiO_2 thin films annealed at various temperatures

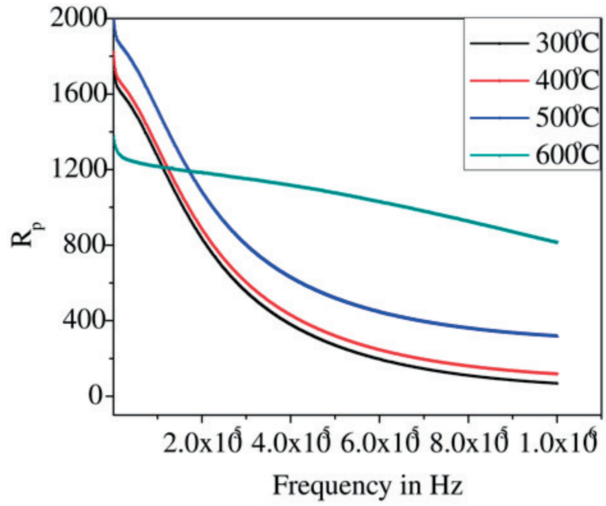


Fig. 6. Parallel resistance versus frequency of MOS devices for TiO_2 thin films annealed at various temperatures

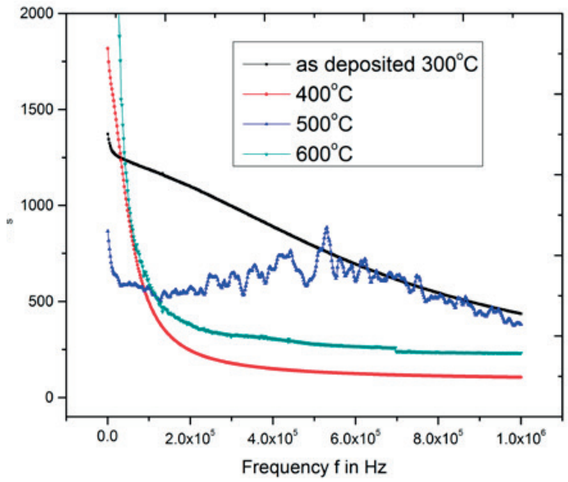


Fig. 7. Series resistance versus frequency of MOS devices for TiO_2 thin films annealed at various temperatures

frequency in Fig. 7. The main findings are that the series resistance exhibits capacitive behavior, beginning high at low frequencies and gradually decreasing with increasing frequency. In comparison to the as-deposited state, the series resistance dramatically drops at 300, 400, 500, and 600 °C, particularly at higher frequencies. The presence of relaxation processes connected to the microstructure alterations in the MOS stack is suggested by the resistance plots' unique peaks at different frequencies. The MOS device's zeta (*Z*) is shown against frequency in Fig. 8. The authors noted that impedance exhibits normal capacitive behaviour, beginning high at low frequencies and decreasing with increasing frequency. The presence of relaxation processes is indicated by the impedance plots unique peaks at different frequencies at 500 °C. The impedance curve exhibits a further decline in magnitude at 600 °C, suggesting a lessening of the capacitive effects. The impedance curve rapidly decreases at higher frequencies at 400 °C, indicating better conductive qualities.

3. Conclusion

At a temperature of 300 °C, the interfacial insulating layers were deposited using the SPD process and subsequently annealed isochronally. The XRD patterns of TiO_2 films observed that, the amorphous structure is absent at 300 °C, while the anatase phase and rutile phase are visible at annealed at 400 °C, 500 °C, and 600 °C. Crystallite sizes increase with annealing temperature, with estimated sizes of 10.62, 13.73, 16.04, and 17.35 nm. SEM grain sizes are consistently greater than XRD, indicating a growing pattern. The EDAX analysis revealed a stoichiometric Titanium (Ti): Oxygen (O) ratio, with a uniform distribution of TiO_2 nano-particles on the surface.

The dielectric characteristics of MOS devices, including tan(δ), conductance, and impedance, were investigated. For (Pt/TiO_2/Si) MOS capacitors, the tan δ – Voltage, *G*/ω – ω, and *Z*-*f* properties were measured. The influence of annealing on the electrical properties of the films is shown

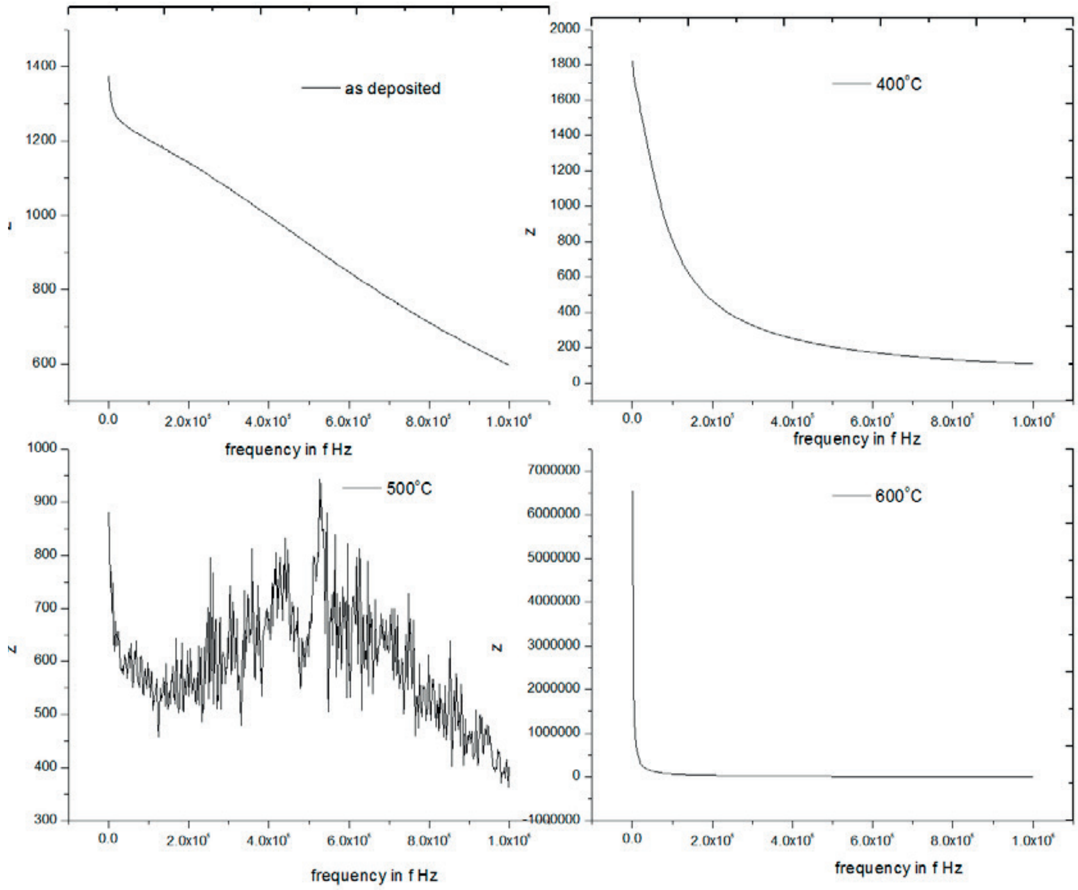


Fig. 8. Zeta (*Z*) versus frequency of MOS devices for TiO_2 thin films annealed at various temperatures

by conductance versus angular frequency study for MOS devices with TiO_2 thin films. Lower conductance at low frequencies and more stable dielectric behaviour at higher frequencies are the results of annealing, which efficiently decreases defects and increases crystalline. The hysteresis loop shows decreased losses due to thermal treatment at 600 °C, which they ascribe to fewer broken bonds and trapped charges at the interface. The parallel resistance decreases rapidly at different temperatures, suggesting thermal activation of charge carriers and changes in the material's electronic properties. The MOS device's series resistance, exhibiting capacitive behaviour, decreasing with frequency, particularly at higher frequencies, compared to the as-deposited state. The MOS device's zeta (*Z*) shows normal capacitive behaviour, with relaxation processes indicated by unique peaks at 500 °C, 600 °C, and 400, with a decline in magnitude at 600 °C and better conductive qualities at 400 °C.

Contribution of the authors

The authors contributed equally to this article.

Conflict of interests

The authors declare that they have no known competing financial interests or personal relationships that could have influenced the work reported in this paper.

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