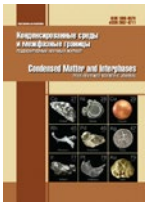

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Noise figure reduction of a GaAs-based pHEMT transistor by optimization of the gate barrier layer thickness using numerical simulation

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Abstract

Objectives: The objective of the present work is to reduce the noise figure of a GaAs-based pHEMT transistor by optimizing the thickness of the gate barrier layer of the transistor heterostructure, and to investigate the applicability of numerical simulation methods for this purpose.

Experimental: Numerical simulation of the transconductance and drain current of a low-noise pHEMT transistor was carried out using the drift-diffusion and hydrodynamic models of charge carrier transport in the channel.

Conclusions: It is shown that the hydrodynamic model describes the experimental results for a pHEMT transistor with a sub-micron gate length more accurately than the drift-diffusion model. The optimal heterostructure design of a low-noise pHEMT transistor was determined by means of the hydrodynamic numerical model, which resulted in a reduction of the minimum noise figure of the pHEMT transistor by 0.1 dB to a level of 0.7 dB.

Keywords: GaAs-pHEMT, Numerical Simulation, Noise figure, Transconductance

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Снижение коэффициента шума pHEMT транзистора на подложке GaAs за счет оптимизации толщины подзатворного барьерного слоя с использованием методов численного моделирования

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Аннотация

Цель статьи: Целью настоящей работы является снижение коэффициента шума pHEMT транзистора на подложке GaAs за счет оптимизации толщины барьерного слоя гетероструктуры транзистора и исследование применимости в данных целях методов численного моделирования.

Экспериментальная часть: Представлены результаты численного моделирования крутизны и тока стока малошумящего pHEMT-транзистора с использованием диффузионно-дрейфовой и гидродинамической моделей транспорта носителей заряда в канале.

Выводы: Показано, что гидродинамическая модель точнее описывает результаты эксперимента для pHEMT-транзистора с затвором субмикронных размеров. С использованием гидродинамической численной модели была определена оптимальная конструкция гетероструктуры малошумящего pHEMT-транзистора, что привело к снижению минимального коэффициента шума pHEMT-транзистора на 0.1 дБ до уровня 0.7 дБ.

Ключевые слова: GaAs-pHEMT, численное моделирование, коэффициент шума, крутизна

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1. Introduction

Pseudomorphic high electron mobility transistors (pHEMT) based on epitaxial heterostructures grown on GaAs substrates have been widely adopted in the production of monolithic microwave integrated circuits for low-noise amplifiers (LNA) [1, 2]. Despite the mature manufacturing technology for such pHEMT transistors, there remains a need for a preliminary numerical calculation of device parameters, which enables the refinement of device designs for specific applications at reduced manufacturing costs.

With the constant development of radio communication technologies, the requirements for the noise figure of LNAs are becoming more demanding, with target values on the order of 1 dB in state-of-the-art systems [3]. The noise figure of an LNA is largely determined by the characteristics of the transistor employed in the device; hence, there is a need to reduce the minimum transistor noise figure N_F to values below 1 dB. In turn, a

reduction of the minimum transistor noise figure is achieved by an increase in the transconductance g in accordance with the following expression [4]:

$$N_F = 1 + \frac{\sqrt{G_{ng} G_{nd}}}{g}, \quad (1)$$

where G_{ng} and G_{nd} are the equivalent noise conductances of a field-effect transistor. Thus, in the development of low-noise pHEMT transistors, the primary design objective is the maximization of the transconductance.

The dependence of the maximum intrinsic transconductance of a pHEMT transistor (excluding the influence of contact pads resistance) on the transistor parameters can be represented by the following analytical expression [5]:

$$g_{\max,\text{int}} = \frac{q\mu n_{s0}}{l_g \sqrt{1 + \left[q\mu n_{s0} \frac{d_{gc} + \Delta d_{gc}}{\varepsilon v_{sat} l_g} \right]^2}}, \quad (2)$$

where q is the elementary charge; m is the electron mobility; n_{s0} is the surface electron concentration in the absence of an external electric field; l_g is the gate length; ε is the dielectric permittivity; d_{gs} is the distance between the gate and the channel layer; Δd_{gc} is the distance between the barrier/channel heterojunction and the electron concentration maximum; v_{sat} is the electron saturation velocity. Among the other heterostructure parameters, it follows from expression (2) that the transconductance is in large part determined by the thickness of the barrier layer, with the dependence $g_{\max,\text{int}} \propto d_{gc}^{-1}$, making it a critical parameter in the optimization of the pHEMT transistor.

Various numerical models, describing the physical phenomena in the transistor with varying degrees of accuracy, can be applied in the calculation of the pHEMT parameters [6]. It should be taken into account that the use of more complex models is associated with greater time and computational costs. Therefore, in the course of transistor development, it is advantageous to employ the simplest models that allow effective calculation of transistor output characteristics with sufficient accuracy. One of the most widely used models not requiring significant computational resources for the numerical calculation of semiconductor device characteristics is the drift-diffusion (DD) model of charge carrier transport, comprising a system of Poisson and continuity differential equations [7]. In this model, it is assumed that the carrier temperature is equal to the crystal lattice temperature, while the carrier mobility is determined by the local electric field strength. However, the use of such an approximation can lead to discrepancies between simulation results and experimental data when gate dimensions are reduced to sub-micron values. At sub-micron gate lengths, velocity overshoot effects occur, associated with electron heating; as a result of this, the effective electron velocity can exceed the saturation velocity [8, 9]. In order to account for these effects, the hydrodynamic (HD) model must be employed, which also includes the calculation of carrier temperature [10]. However, since the HD model is more complex compared to the DD model, its use is associated with increased time and computational requirements.

The objective of the present work is to reduce the noise figure of a GaAs-based pHEMT transistor by optimizing the thickness of the gate barrier layer of the transistor heterostructure, and to investigate the applicability of numerical simulation methods for this purpose.

2. Experimental

The reference transistor structure investigated in the present study is the pHEMT130, which features a gate barrier layer thickness of 13 nm and was designed for operation under negative bias voltage. The pHEMT130 transistor heterostructure with an InGaP etch-stop layer was grown by molecular beam epitaxy on a semi-insulating GaAs (001) 3-inch substrate. The contact layer of the heterostructure consists of GaAs with a thickness of 54 nm and a Si doping concentration of $3.0 \cdot 10^{18}$ cm^{-3}. Below the contact layer are the following: an $Al_{0.23}Ga_{0.77}As$ sacrificial etch barrier layer with a thickness of 10.5 nm; an $In_{0.51}Ga_{0.49}P$ etch-stop layer with a thickness of 3 nm; an $Al_{0.23}Ga_{0.77}As$ barrier layer with a thickness of 13 nm; a Si delta-doping region with a surface concentration of $2.1 \cdot 10^{12}$ cm^{-2} incorporated within a 0.8 nm GaAs layer; and AlGaAs and GaAs spacer layers with thicknesses of 7 nm and 1.5 nm, respectively. The channel layer consists of an $In_{0.23}Ga_{0.77}As$

ternary solid solution with a thickness of 10 nm. The described functional layers were grown on an AlGaAs/GaAs buffer heterostructure. The substrate temperature during epitaxial growth was varied from 560 °C for AlGaAs and GaAs layers to 500 °C for InGaAs and InGaP layers, with a III/V material flux ratio of 1/10.

The transistor design, schematically illustrated in Fig. 1, was formed by etching the upper layer region beneath the gate, with the etch depth limited by the depth of the InGaP etch-stop layer. The gate length of the transistor is 0.25 μm with a gate width of 240 μm. The distance between the drain and source contacts is 2.50 μm. The gate contact metallization was formed by deposition of Ti/Pt/Au metal layers with thicknesses of 30/7/300 nm, respectively. The ohmic contacts consist of multilayer Ge/Au/Ni/Au metallization with thicknesses of 20/50/15/150 nm. Silicon nitride passivation was deposited by means of plasma-enhanced chemical vapor deposition.

In order to evaluate the transistor parameters during simulation, the drain current I_d was calculated at a constant drain contact voltage as a function of the applied gate voltage U_g. The transconductance was determined by the expression $g_m = \partial I_d / \partial U_g$. Transistor parameter simulation was carried out using the DD and HD models implemented in the Silvaco TCAD software. The use of the DD model is more advantageous given the small deviations in the results, due to the simpler calculation procedure. In this model, the solution of the differential equations yields the carrier concentrations and the electric potential values at the mesh nodes of the transistor model. In addition, simulation was performed using the HD model in the transistor channel region, which incorporates carrier temperature into the calculation in addition to the DD model parameters. Both models account for the dependence of carrier mobility on the doping concentration [11] and carrier velocity saturation in high electric fields. Calculations were performed using Fermi-Dirac statistics. The effects of Shockley-Read-Hall recombination, Auger recombination, and radiative recombination processes in direct-bandgap semiconductors were taken into account.

The material parameters used in the model are those characteristic of bulk materials. The position of the conduction band minimum in the heterostructure layers is determined relative to the electron affinity of GaAs. The numerical transistor model was calibrated using parameters obtained from experimental data. One such calibration parameter was the Schottky barrier height, which determines the pinch-off voltage. In the DD model, the electron saturation velocity in the InGaAs channel was adjusted to match data obtained from real transistors with short gate lengths [9]. In the HD model, which accounts for the velocity overshoot effect, a calibration

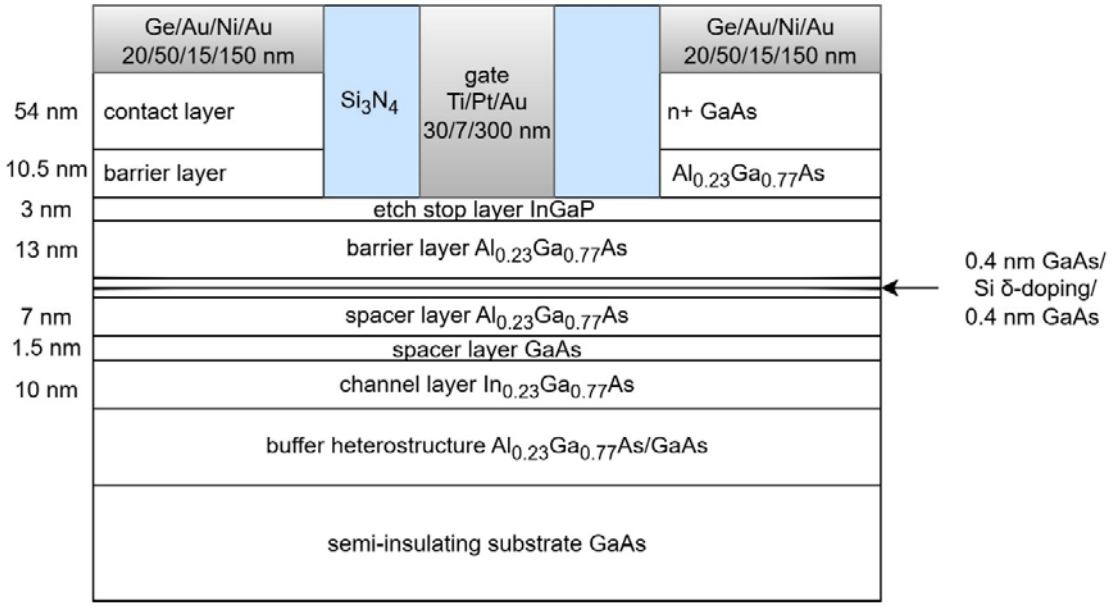

Fig. 1. Scheme of pHEMT130 heterostructure

carrier relaxation time in InGaAs was used in the approximation of a constant parameter value on the order of tenths of a picosecond [12]. The main parameters used in the model are presented in Table 1.

3. Results and discussion

The fabricated transistors were measured in a 50-Ω transmission line without impedance transformers at room temperature, with the noise figure measured at a frequency of 3 GHz. According to the measurement results, the peak transconductance of the fabricated pHEMT130 transistor reached 498 mS/mm, the drain current at zero gate voltage was 278 mA/mm, and the noise figure was 0.8 dB.

Based on the experimental data, numerical transistor models were developed using the DD and HD approaches to charge carrier transport. As can be seen from the comparison of measurement and simulation results presented in Fig. 2, the calculated characteristics of both models agree reasonably well with the measurement results in the voltage range below −0.4 V. However, in the voltage range above −0.4 V, the DD model simulation results demonstrate a smoother transconductance profile compared to the measurement results. Given that the peak transconductance value in the calculated profile differs significantly from the experimental values when the DD model is used, the assessment of the influence of heterostructure design

Table 1. Values of the model's main parameters

Parameter	GaAs	AlGaAs	InGaP	InGaAs
Dielectric constant [13]	12.9	12.25	11.8	13.29
Effective mass [13]	$0.063m_0$	$0.082m_0$	$0.088m_0$	$0.053m_0$
Electron affinity, eV [13]	4.07	3.88	3.87	4.26
Band gap, eV [13]	1.424	1.711	1.849	1.100
Electron saturation velocity, 10^7 cm/s [14]	0.72	0.74	0.74	0.73 (HD model) 2.28 (DD model)
Charge carrier relaxation time, ps	–	–	–	0.3
Schottky barrier height, eV	4.73			
Specific ohmic contact resistance, Ω·cm^2	$2\cdot10^{-6}$			
Surface charge density at the semiconductor/dielectric interface, cm^{-2} [15]	$4\cdot10^{11}$			

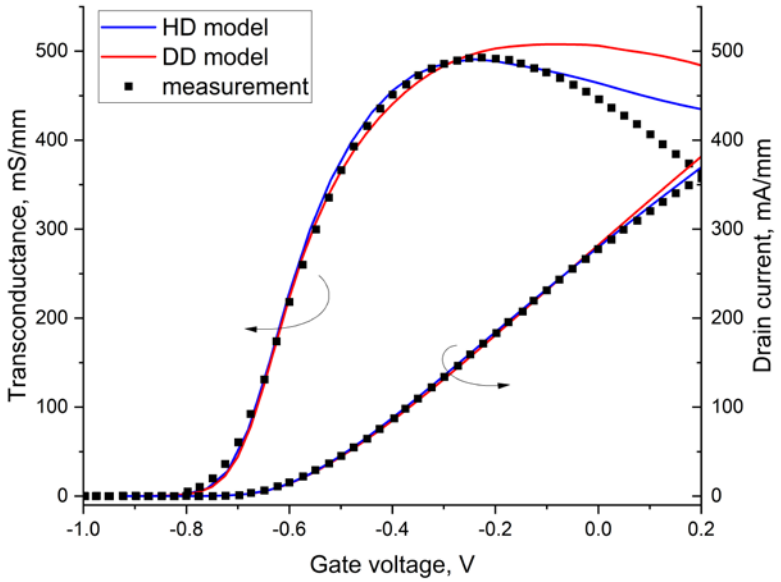

Fig. 2. Simulation and measurement results of the pHEMT130 transistor characteristics using DD and HD models

changes on the peak transconductance would be incorrect. Furthermore, the deviation of the bias voltage corresponding to the transconductance maximum does not allow for the design of a transistor targeting the required operating conditions in an LNA circuit. A higher degree of agreement is achieved when the HD transport model is used in the transistor channel, which simulates the velocity overshoot effect and thus provides an accurate description of the most important voltage range corresponding to the peak transconductance. However, when the voltage is varied toward positive values, the model does not adequately describe the abrupt drop in transconductance values. This observation may be attributable to a stronger spatial confinement of electrons in the channel than assumed in the model, arising from the quantization of energy levels [16]. Nevertheless, the employed model can be successfully applied to calculate the peak transconductance.

In order to improve the heterostructure design, the dependences of the transistor parameters on the gate barrier layer thickness were calculated using the HD model. As follows from Fig. 3, the obtained calculated data demonstrate an increase in the peak transconductance value with a decrease in the gate barrier layer thickness. At the same time, the voltage corresponding to the peak transconductance also shifts toward positive values. In the optimization of the heterostructure design of the investigated transistor, the transconductance maximum should remain in the negative voltage region, since a shift of the transconductance maximum into the positive voltage region necessitates changes to circuit design solutions in amplifier development, requiring the use of an additional voltage source providing dual-polarity supply.

Based on the calculated data, a barrier thickness of 10.5 nm was selected to achieve a higher peak transconductance in the improved pHEMT105 transistor. According to the simulation results at this barrier thickness, the transconductance maximum is achieved at a gate-source voltage of −0.06 V. The small negative gate bias is needed to ensure a sufficient technological margin.

As follows from the comparison of the calculated and measured static parameters of the fabricated transistors presented in Fig. 4, the simulation results allow for a sufficiently accurate description of the effect of pinch-off voltage shift and the increase in peak transconductance with a decrease in the gate barrier region thickness. According to the measurement results of the pHEMT105, the peak transconductance was increased to 517 mS/mm compared to the pHEMT130, while the current density decreased to a level of 200 mA/mm. The obtained value of N_F was 0.7 dB, which is 0.1 dB lower than the

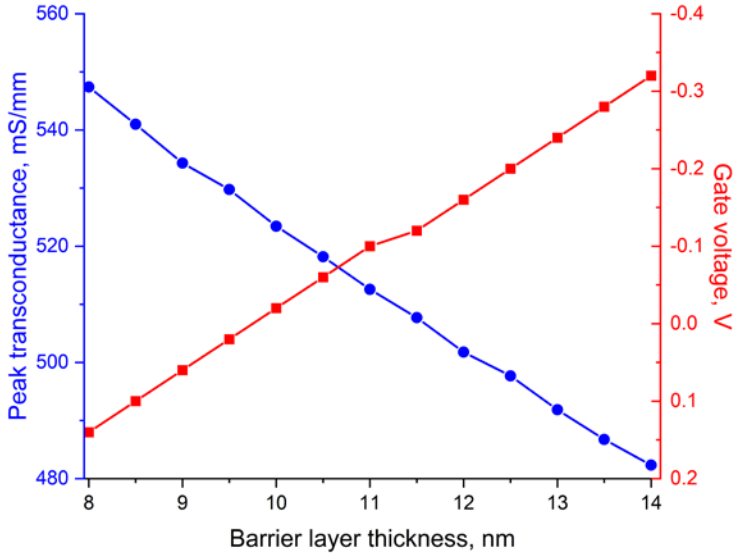

Fig. 3. Calculated dependencies of the transistor peak transconductance and the corresponding voltage on the gate barrier layer thickness

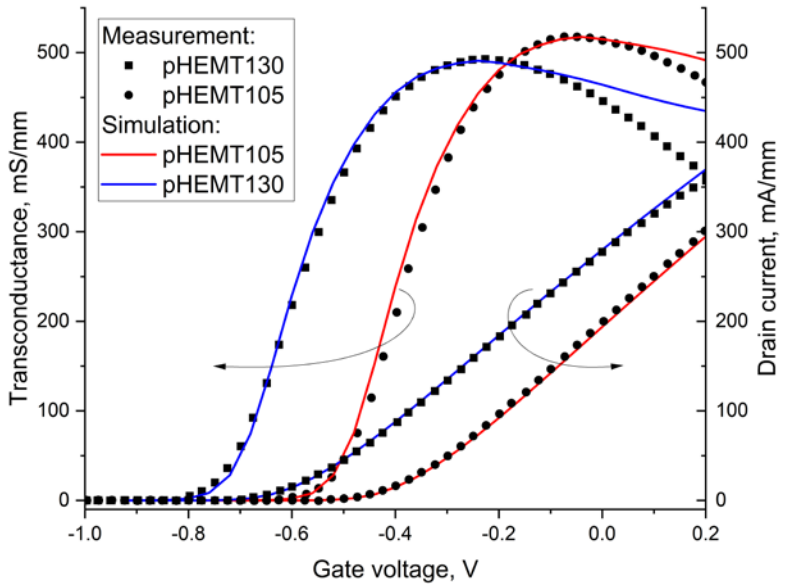

Fig. 4. Simulation and measurement results of the pHEMT130 and pHEMT105 transistors using the HD model

corresponding characteristic of the pHEMT130. The achieved reduction in N_F is significant in the development of ultra-low-noise amplifiers with a device noise figure below 1 dB, which confirms the effectiveness of the applied methodology. At the same time, the record N_F values of state-of-the-art pHEMT transistors with sub-micron gates on GaAs substrates are below 0.3 dB [17], which indicates the potential for further improvement of the developed pHEMT transistor designs. Taking into account that a reduction in the gate barrier layer thickness by 2.5 nm, in addition to the shift in the operating voltage range, leads to a decrease in the saturation current by 78 mA/mm, further reduction of the thickness may result in a critical decrease in the output power. Therefore, further optimization pathways for the transistor design are associated with the doping and channel layer parameters, as well as the technology of gate contact formation.

4. Conclusions

In the present work, the gate barrier layer thickness of a low-noise pHEMT transistor heterostructure was optimized by means of numerical simulation methods in order to reduce the noise figure.

It is shown that the drift-diffusion model of charge carrier transport allows one to predict the transconductance values of a pHEMT transistor with a gate length of 250 nm only in a limited range of reverse voltages not exceeding -0.4 V. At the same time, the hydrodynamic model describes the experimental drain current and transconductance values of the transistor with high accuracy over the entire operating range of reverse voltages.

In order to achieve the maximum transconductance and, consequently, the minimum noise figure of the low-noise pHEMT transistor, the optimal barrier layer thickness in the pHEMT heterostructure design was determined on the basis of the hydrodynamic model. Thus, as a result of reducing the gate barrier region thickness from 13 nm to the calculated value of 10.5 nm, the minimum noise figure of the transistor was reduced by 0.1 dB and reached a level of 0.7 dB.

Authors' contributions

The authors contributed equally to this article.

Conflict of interests

The authors declare that they have no known competing financial interests or personal relationships that could have influenced the work reported in this paper.

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